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DIGITAL DESIGN OF THE LHC LOW LEVEL RF: THE TUNING SYSTEM FOR THE SUPERCONDUCTING CAVITIES

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Abstract

The low level RF systems for the LHC are based extensively on digital technology, not only to achieve the required performance and stability but also to provide full remote control and diagnostics facilities needed since most of the RF system is inaccessible during operation. The hardware is based on modular VME with a specially designed P2 backplane for timing distribution, fast data interchange and low noise linear power supplies. Extensive design re-use and the use of graphic FPGA design tools have streamlined the design process. A milestone was the test of the tuning system for the superconducting cavities. The tuning control module is based on a 2M gate FPGA with on-board DSP. Its design and functionality are described, including features such as automatic cavity measurements. Work is ongoing on completion of other modules and building up complete software and diagnostics facilities.

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INTRODUCTION

The LHC RF System

The RF system for the LHC consists of 16 super-conducting 400MHz cavities, eight per ring. Each is driven by a 300 kW CW klystron through a variable power coupler. For each cavity the RF voltage, phase, tuning and coupling must be precisely controlled for all beam conditions. Individual wideband and narrowband feedbacks are needed to minimize impedance and noise. Beam feedback and synchronization systems are also needed.

Digital Low Level RF

Digital technology, largely FPGA based, will be used as far as possible in LHC, to achieve high performance and stability, and provide the full remote control and diagnostics facilities needed. While very successful digital implementations have recently been done for the LEIR RF system [1] and Linac upgrades [2] and digital filtering has long been used in SPS beam control [3], the LHC is the first of CERN's large accelerators to make such extensive use of digital technology in its RF system.

CAVITY CONTROLLER LAYOUT

Controls and feedback systems [4] for each cavity are housed in a VME based cavity controller. The loops comprise: cavity tuning, RF feedbacks, klystron ripple compensation and cavity conditioning.

16 bit VME data transfer being more than adequate, the P2 connector is freed for a specially designed backplane to handle fast data interchange, timing distribution and additional power lines for RF circuits [5].

MODULE DESIGN & FEATURES

Tools & Design-flow

For a project of this size, (12 VME modules in the cavity controller alone) issues such as reliability, design re-use and full design check-out before production are fundamental. These are reflected in the choice of design and development tools and in the test methodology.

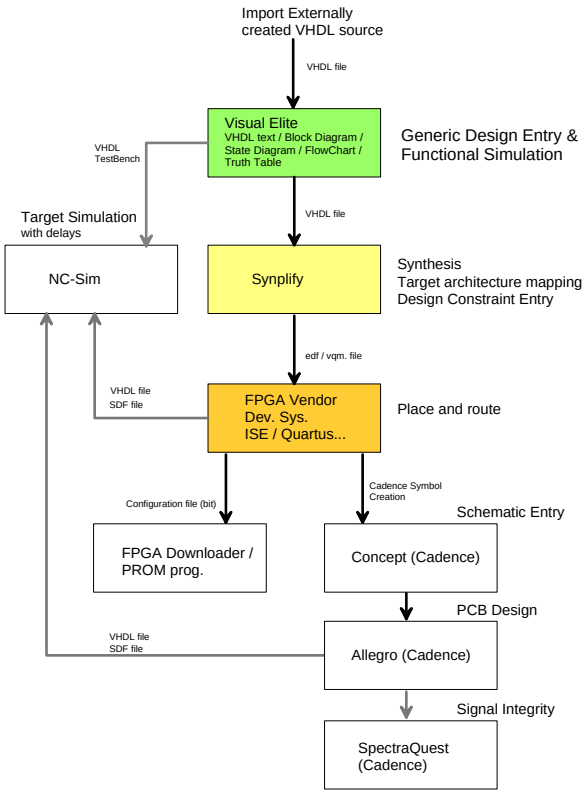

Figure 1: Design Flow

The design tool set chosen ranges seamlessly from development of the FPGA code right down to the circuit board [6]. FPGA code is developed with Visual Elite. It graphically and textually aids the designer to enter and verify generic reusable VHDL code. Block diagrams relieve the designer from laborious VHDL interconnect syntax and simplify verification. Visual also offers a powerful functional simulator with graphically created wave-form stimuli. Design or module reuse is simplified by access to other projects via the library browser.

Finally Visual Elite generates a single VHDL flat file which is translated by the Synplicity synthesizer into elementary FPGA target architecture blocks. The synthesizer offers constraint entry, with constraint driven optimisation, greatly improving the design performance.

The place and route phase is done in the FPGA manufacturer development system e.g. Xilinx ISE. FPGA pin constraints are entered here. PCB design flow is done in Cadence; which can automatically build custom FPGA symbols from files generated by the place and route tool, essential in view of the dense FPGA packages used. Cadence also offers a sound environment to deal with PCB impedance requirements for RF and fast signals.

Module Memory Map

The LHC RF Low Level crate offers space for up to 15 RF modules in 16 Mb address space. Most modules carry post-mortem and observation memories of 256k x 16b, storing 64 LHC machine turns of data at 40 Ms/s (LHC bunch rate). The Module memory footprint is fixed at 1 Mb, allowing a complete memory to be mapped in half this space, the remainder left available for miscellaneous registers and FPGA resident memories. The memory map is created in an Excel file. It includes all details for the software team to develop drivers and higher level code. The Excel file also serves to create a VHDL package containing all symbolic address constants, used throughout the FPGA code, greatly simplifying management of address changes.

CAVITY TUNING SYSTEM

The cavity has a mechanical tuning system driven by a stepping motor. The tuning system uses two RF signals, the cavity field measured by an antenna and the drive measured by directional coupler on the input waveguide. Scaling ensures that the tuning is independent of field and power levels. The control module is shown in figure 2. It is based on a 2M gate FPGA with on-board Tiger Sharc DSP. The antenna signal and the drive are mixed with a 380 MHz local oscillator to generate 20MHz IFs that are fed into 14 bits ADCs clocked at 80MHz. Digital I/Q demodulators then generate (I,Q) pairs at the 40MHz rate. After decimation, two signals (error signal and scaling factor) are generated at the 9.766kHz rate, to be used by the DSP.

FPGA – DSP Bridge

The FPGA is connected to the DSP by a 32bit bidirectional data bus, 11 address lines, control and IRQ lines. Only the lower 16 bits are used by the FPGA. The bridge implementation is made to maximally decouple the devices. Firstly the same clock is used for the FPGA and DSP, allowing synchronous zero wait-state data transfers. Secondly the DSP is the sole master. FPGA resident DSP registers are read-only to the FPGA if writable by the DSP and vice-versa. The FPGA implements two 1k x 16b, bi-directional data exchange DSP memory buffers. In operation, one DSP interrupt-line is triggered at regular 8 ms intervals, to signal data present for the DSP. The DSP interrupt treatment is steered by a DSP command register writable from the FPGA.

Memory Implementation

The module carries eight 256k x 16b synchronous SRAM chips, in 2 banks each of 4 chips for the I/Q decoded components from four 80 Ms/s ADC channels. The FPGA interleaves I and Q words in each bank. The Post-Mortem (PM) memory bank continuously stores I/Q channel data at the full data-rate and recording can only be halted by a hardware PM trigger. The Observation memory bank records the data at a rate selected by an VME ORS register and can be stopped by a hard or software trigger. ORS also controls a filter which averages I/Q data inside the accumulation interval. Each memory has its own data bus while each bank shares the address bus. Memory data can be read-back once the recording is halted: the address bus is switched from the

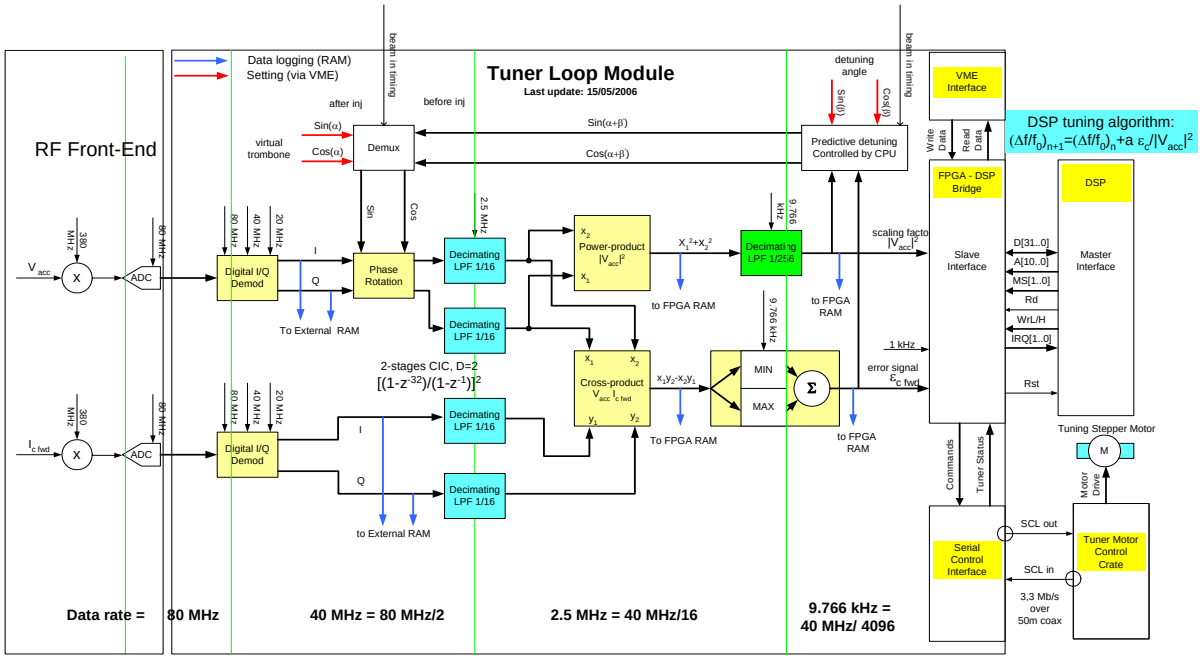

Figure 2: The LHC RF Cavity Tuning System.

write address counter to the VME address and the data bus of the entire bank is inversed. A view port control nibble selects the memory data bus to be read by the VME addressed memory view-port

Special FPGA Implementations

Figure 3 shows a 2 stage CIC decimating filter implementation. Here eight of these filters are used to smooth I/Q data over 16 samples, at the same time nulling out the effect of ADC DC offsets passing from the digital I/Q demodulator. The entire filter is clocked at 40MHz but the input and output rates can operate at lower frequencies allowing this filter to be cascaded. This generic implementation is valid if the ratio between input and output rate is 16. Other ratios will change the gain and the bit-growth [7].

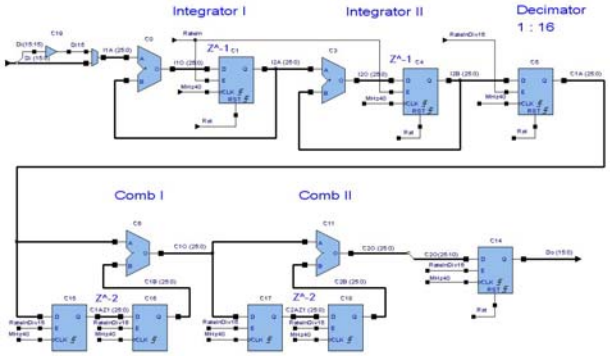

Figure 3: Two Stage Decimating CIC LP Filter

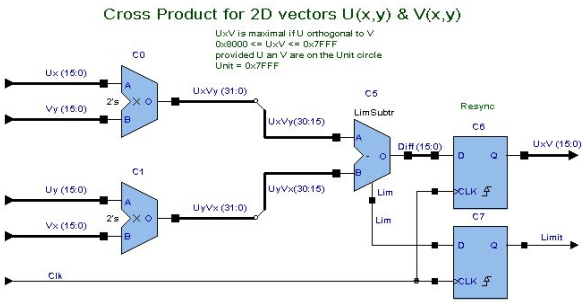

Figure 4: Cross Product

Figure 4 shows a 2-dimensional cross-product implementation to compute an error signal proportional to the sine of the phase between the antenna and the cavity drive signals. To make tuning independent of cavity voltage, the product of the moduli of both vectors is afterwards normalized in the DSP by dividing by $|Vacc|^2$. (See figure 2). The output adder is custom implemented and overflow tolerant. This implementation requires just 2 embedded multipliers.

Diagnostics & measurements

Thanks to the normalization, the error signal varies linearly with tuner displacement over the full mechanical range, ensuring lock-in from all positions. Code for automatic measurements, such as the cavity tune and transient response has been built into the FPGA and DSP. A tune command sweeps the tuner through its range, measuring and storing values in the observation buffer. Figure 5 shows tuning plots derived from data read back, for two positions of the variable coupler.

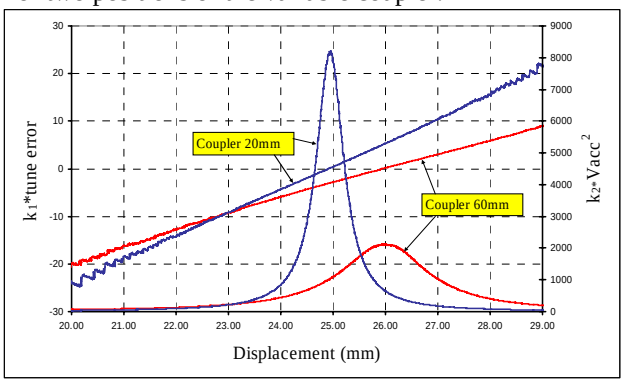

Figure 5: Automatic Tuning Measurements.

SOFTWARE

Clear definition of the hardware interface via the memory map has proved essential in smooth build-up of drivers and software under CERN's Front End Software Architecture (FESA). For each new module the memory map is used to build the driver and a menu driven application for hardware debugging and system test. [5] Standard tools will be used for remote monitoring and diagnostics. Interfaces will be provided for building LabView and MATLAB expert applications.

CONCLUSIONS

The choices of hardware and digital design and development tools for the LHC low level RF system have been validated in the construction and test of the tuning system. Thanks to careful and rigorous approach, design efficiency and hardware reliability are at the levels required. Inherent advantages of the digital approach, such as full remote control and flexible diagnostics facilities, have also been clearly demonstrated.

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